UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,959,088 B1
APPLICATION NO. : 09/527691
DATED : October 25, 2005
INVENTOR(S) : Masahiko Yamaguchi

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Drawings,
Sheet 3, FIG. 3, "ANALYSE" should read -- ANALYZE --.
Sheet 4, FIG. 4, "ANALYSE" should read -- ANALYZE --.
Sheet 7, FIG. 7, "ANALYSE" should read -- ANALYZE --.
Sheet 10, FIG. 10, "ANALYSE" should read -- ANALYZE --.
Sheet 11, FIG. 11, "ANALYSING" should read -- ANALYZING --.
Sheet 12, FIG. 12, "ANALYSE" should read -- ANALYZE --.

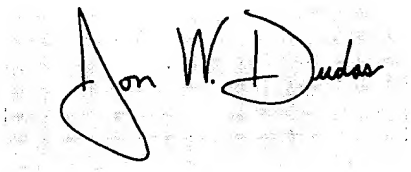
Column 6,
Line 4, "form" should read -- from --.

Column 7,
Lines 10 and 29, delete "a".

Column 8,
Line 17, "a" should read -- at --.
Line 47, "step;" should read -- step, wherein the predetermined bit positions are a predetermined number of upper bit positions; --.
Line 51, "step," should read -- step. --.
Lines 52 and 53, should be deleted.

Signed and Sealed this

Twenty-seventh Day of June, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office